DATA SHEET

SZA1010
Digital Servo Driver 3 (DSD-3)

Preliminary specification
File under Integrated Circuits, IC01

1997 Apr 07

Philips
Semiconductors

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Digital Servo Driver 3 (DSD-3) SZA1010

FEATURES

Servo functions

- 1-bit class-D focus actuator driver (4 Ω)
- 1-bit class-D radial actuator driver (4 Ω)
- 1-bit class-D sledge motor driver (2 Ω).

Other features

- Supply voltage 5 V only
- Small package (SOT163-1)
- Higher efficiency, compared with conventional drivers, due to the class-D principle
- Built-in digital notch filters for higher efficiency
- Enable input for focus and radial driver
- Enable input for sledge driver
- 3-state input for radial driver
- Doubled clock frequency
- Differential outputs for all drivers
- Separate power supply pins for all drivers.

GENERAL DESCRIPTION

The SZA1010 or Digital Servo Driver 3 (DSD-3) consists of 1-bit class-D power drivers, which are specially designed for digital servo applications. Three such amplifiers are integrated in one chip, to drive the focus and radial actuators and the sledge motor of a compact disc optical system.

The main benefits of using this principle are its higher efficiency grade compared to conventional analog power amplifiers, its higher integration level, its differential output and the fact that only a few external components are needed. When using these digital power drivers in a digital servo application, the statement ‘complete digital servo loop’ becomes more realistic.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DDD}	digital supply voltage	4.5	–	5.5	V
$V_{DDA(F)}$	analog supply voltage focus actuator	4.5	–	5.5	V
$V_{DDA(R)}$	analog supply voltage radial actuator	4.5	–	5.5	V
$V_{DDA(S)}$	analog supply voltage sledge actuator	4.5	–	5.5	V
I_{DDDq}	quiescent digital supply current	–	–	10	µA
$I_{DDA(F)}$	analog supply current focus actuator	–	126	250	mA
$I_{DDA(R)}$	analog supply current radial actuator	–	20	250	mA
$I_{DDA(S)}$	analog supply current sledge actuator	–	150	560	mA
$f_{i(clk)}$	input clock frequency	–	8.4672	10	MHz
P_{tot}	total power dissipation	–	tbf	–	mW
T_{amb}	operating ambient temperature	–40	–	+85	°C

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
SZA1010T	SO20	plastic small outline package; 20 leads; body width 7.5 mm	SOT163-1

BLOCK DIAGRAM

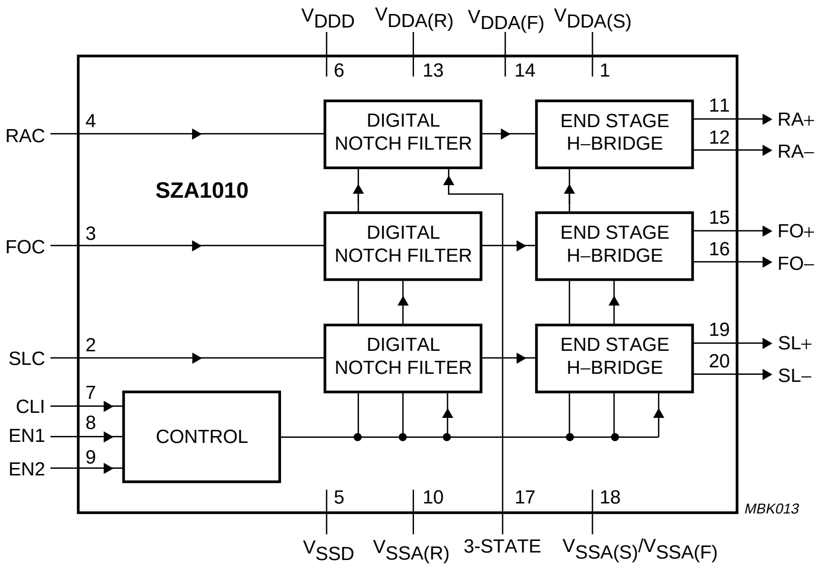


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
$V_{DDA(S)}$	1	analog supply voltage for sledge motor driver
SLC	2	PDM input for sledge driver
FOC	3	PDM input for focus driver
RAC	4	PDM input for radial driver
V_{SSD}	5	digital ground
V_{DDD}	6	digital supply voltage
CLI	7	clock input
EN1	8	enable input 1
EN2	9	enable input 2
$V_{SSA(R)}$	10	analog ground for radial driver
RA+	11	radial driver (positive output)
RA–	12	radial driver (negative output)
$V_{DDA(R)}$	13	analog supply voltage for radial driver
$V_{DDA(F)}$	14	analog supply voltage for focus
FO+	15	focus driver (positive output)
FO–	16	focus driver (negative output)
3-STATE	17	radial 3-state input
$V_{SSA(S)}$/ $V_{SSA(F)}$	18	analog ground for sledge driver/focus
SL+	19	sledge driver (positive output)
SL–	20	sledge driver (negative output)

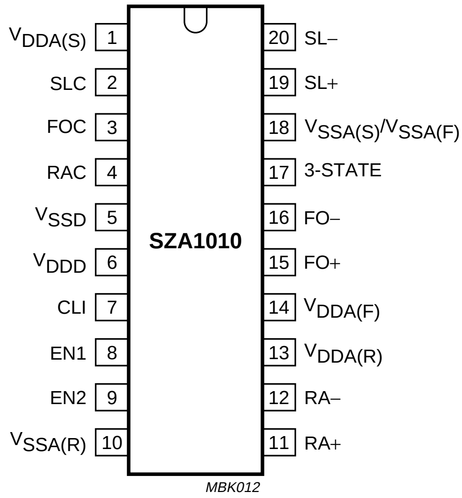


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

Principle of a class-D digital power driver

Figure 3 shows the block diagram of one of the digital drivers integrated in the DSD-3. It consists of a timing block and four CMOS switches. The input signal is a 1-bit Pulse Density Modulated (PDM) signal, the output of the digital servo ICs.

The maximum operating clock frequency of the device is 10 MHz. In combination with most frequently used Philips digital servo ICs, the operating frequency of the digital drivers is 8.4672 MHz (192 × 44.1 kHz). The sampling frequency of the 1-bit code however is 2.1168 MHz, so internally in the DSD-3 the clock speed of the switches will be 2.1168 MHz.
The higher input clock frequency is used to make non-overlapping pulses to prevent short-circuits between the supply voltages. For the control of the switches, two states can be distinguished. If the 1-bit code contains a logic 1, switches A and D are closed and current will flow in the direction as shown in Fig.4.

If the 1-bit code contains a logic 0, switches B and C are closed and current will flow in the opposite direction, as shown in Fig.5.

This indicates that the difference between the mean number of ones and zeros in the PDM signal determines the direction in which the actuator or motor will rotate.

If the mean number of ones and zeros is equal (Idle mode) the current through the motor or actuator is alternated between the positive and negative direction at a speed of half the sample frequency of 2.1168 MHz. This results in a high dissipation and the motor does not move.

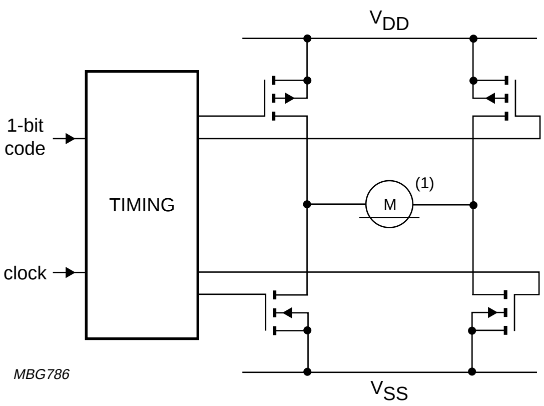
To improve the efficiency, a digital notch filter is added at the input of the digital drivers. This filters the Idle mode pattern (1010101010 etc.) see Fig.6.

The amplitude transfer as a function of frequency is given in Fig.7.

Figure 7 shows that the filter has a zero on $\frac{1}{2}f_s$, thereby filtering out the Idle pattern (101010). The output of this filter is a three-level code (1.5-bit). For the control of the switches three states (1.5-bit) can be distinguished: the two states as described earlier and a third one. This state is used when an idling pattern is supplied.

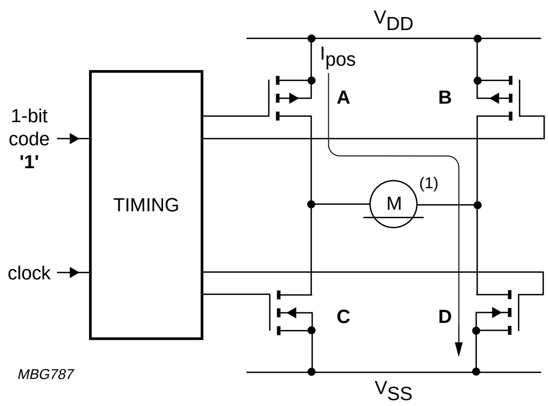
Switches C and D are closed (see Fig.8). In this Idle mode, no current will flow and thus the efficiency will be improved. This mode is also used to short-circuit the inductive actuator/motor. In this way, high induction voltages are prevented because the current can commutate via the filter and the short-circuit in the switches. All three drivers (radial, focus and sledge) contain a digital notch filter as described (see Fig.6). Each driver has its own power supply pins to reduce crosstalk due to of the relative high current flowing through the pins.

Compared to the DSD-2, the DSD-3 has a 3-state mode for the radial output, which is useful when active damping of the radial actuator is needed. When fast access times are required, the sledge has to move with high accelerations. To prevent the radial actuator from moving too far from its centre position due to the acceleration, active damping is applied. In order to measure the displacement of the radial actuator, the voltage induced by the actuator itself is measured, which is proportional to its speed. The damping consists of a sequence of controlling, waiting, measuring and controlling etc. To be able to measure the induced voltage properly, the influence of the DSD-3 is eliminated by switching it into 3-state mode.



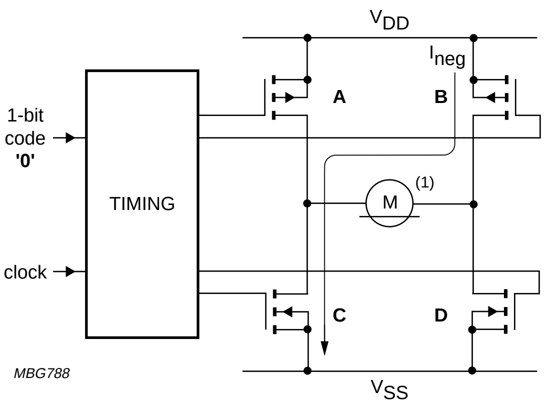
(1) Sledge motor; focus/radial motor.

Fig.3 One of the digital drivers.



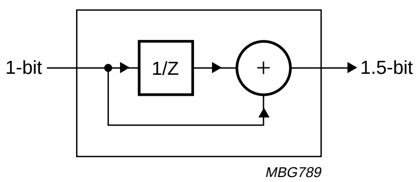
(1) Sledge motor; focus/radial motor.

Fig.4 1-bit code is logic 1.



(1) Sledge motor; focus/radial motor.

Fig.5 1-bit code is logic 0.



The filter consists of a simple delay element (flip-flop) and an adder. The transfer from input-to-output is: $H(z) = 1 + z^{-1}$.

Fig.6 Notch filter at input of digital drivers.

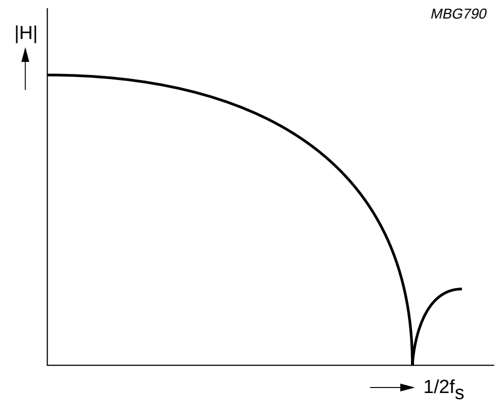
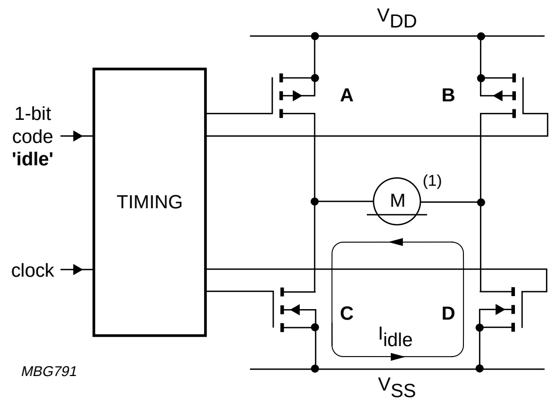


Fig.7 Amplitude transfer.



(1) Sledge motor; focus/radial motor.

Fig.8 Idling pattern.

Switches

The digital part of the power drivers consists of standard cells. The power switches are specifically designed for CD applications. The most important feature is their on-resistance. In the applications, they have to drive very low-ohmic actuators and/or motors. The switches are designed to have an on-resistance of 2 Ω for the actuator drivers and 1 Ω for the sledge motor driver. In any mode, there are always two switches in series with the actuator/motor. The total loss due to the switches is 4 Ω for the actuators and 2 Ω for the sledge motor.

3-state input

When the 3-STATE input (pin 17) is made HIGH, the four CMOS switches of the radial driver are opened. Consequently, the radial output pins RA+ (pin 11) and RA– (pin 12) switch into a high impedance state.

To set the circuit into 3-state mode, the clock signal (CLI) is not required; the 3-STATE input is a direct, asynchronous input. It has an internal pull-down resistor.

Timing of input and output signals

All internal timing signals are derived from the externally supplied CLI signal.

Sampling of the data inputs (SLC, FOC and RAC) occurs at a frequency of $\frac{1}{4}$CL. For each channel, the clocking-in occurs at a different positive edge of CLI. Because there are only 3 channels, and the clock frequency CLI is divided-by-4, only 3 out of 4 positive edges are effective for sampling one of the inputs.

The switching of the outputs occurs in a similar way, except that in this event the negative edge of CLI is used. In this way, the input signals are immune to the noise radiated by the switching of the outputs. It is possible that an output transition will have a noticeable effect on the power supply voltage or the ground voltage. To avoid simultaneous transitions of all outputs, the outputs of each bridge are also clocked at a different phase of CLI. Consequently there are only 3 out of 4 negative edges effective.

To reset the circuit, both the reset condition and the clock should be present, because all flip-flops are reset synchronously. The clock signal is also required to obtain one of the possible modes of operation indicated in Table 1.

Table 1 Possible modes of operation

EN1	EN2	SLEDGE DRIVER	FOCUS/RADIAL DRIVER	MODE
0	0	off	off	standby
0	1	off	on	partly operating
1	0	off	off	reset
1	1	on	on	operating

The timing diagram as shown in Fig.9 gives the relationship between the different clocks.

The negative edge of the signals called ncl0 to ncl2 is used to process the incoming data (see Table 2).

The negative edge of all signals called cl0s to cl2s is used to trigger the outputs (see Table 2).

Table 2 Signals ncl0 to ncl2 and cl0s to cl2s

SIGNAL	DESCRIPTION
ncl0	sledge input sampling clock
ncl1	focus input sampling clock
ncl2	radial input sampling clock
cl0s	sledge output trigger clock
cl1s	focus output trigger clock
cl2s	radial output trigger clock

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DDD}	digital supply voltage	–0.5	+6.5	V
$V_{DDA(x)}$	analog supply voltage	–0.5	+6.5	V
$V_{SSD} - V_{SSA(x)}$	ground supply voltage difference	–5	+5	mV
P_{tot}	total power dissipation	–	tbf	mW
T_{stg}	storage temperature	–55	+150	°C
T_{amb}	operating ambient temperature	–40	+85	°C

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient in free air	75	K/W

CHARACTERISTICS

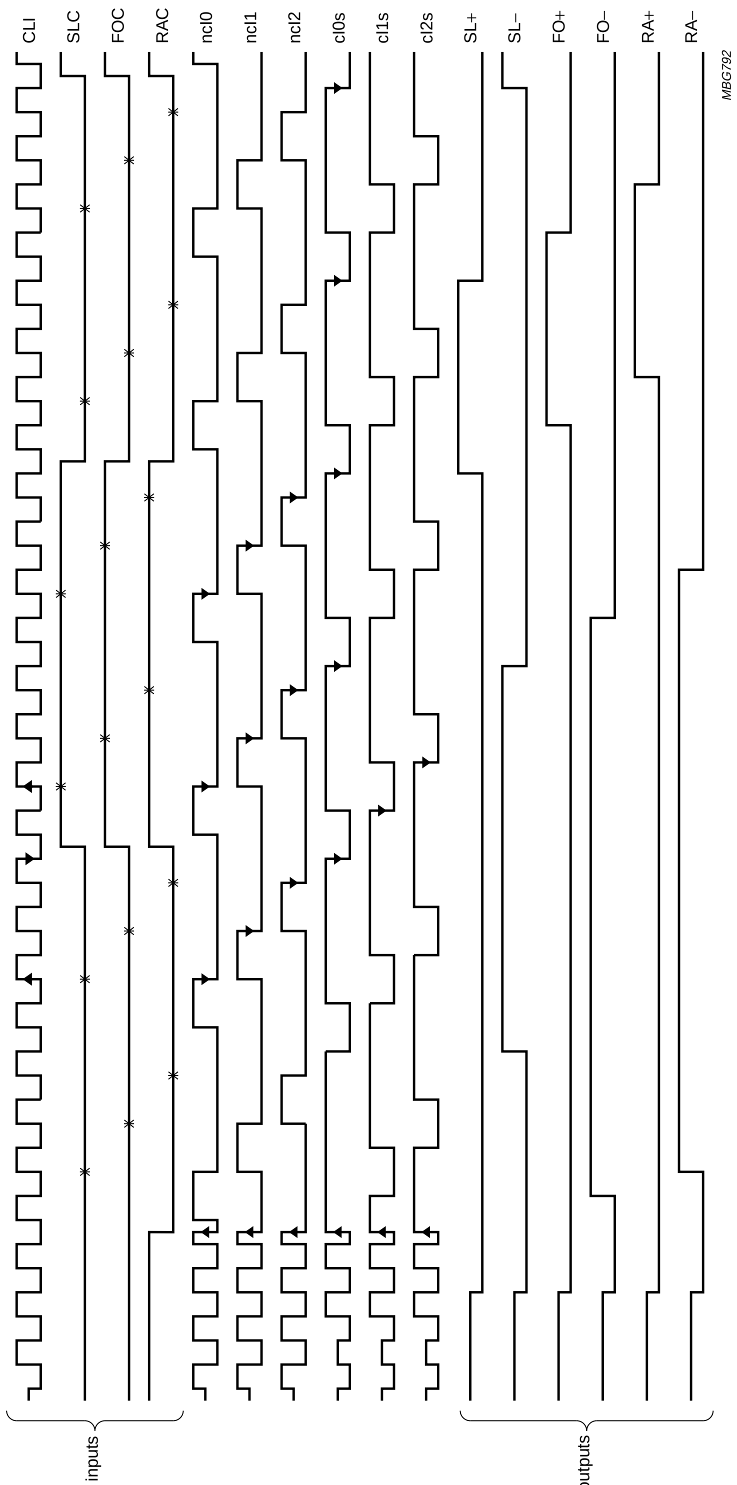
$V_{DDD} = V_{DDA(x)} = 5$ V; $V_{SSD} = V_{SSA(x)} = 0$ V; $T_{amb} = 25$ °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
General						
V_{DDD}	digital supply voltage		4.5	–	5.5	V
$V_{DDA(x)}$	analog supply voltage		4.5	–	5.5	V
I_{DDDq}	quiescent digital supply current		–	–	tbf	μA
$I_{DDA(F)(max)}$	maximum analog supply current focus actuator	note 1	–	126	250	mA
$I_{DDA(R)(max)}$	maximum analog supply current radial actuator	note 1	–	20	250	mA
$I_{DDA(S)(max)}$	maximum analog supply current sledge actuator	note 1	–	150	560	mA
$f_{i(clk)}$	input clock frequency		–	8.4672	10	MHz
P_{tot}	total power dissipation		–	tbf	–	mW
T_{amb}	operating ambient temperature		–40	–	+85	°C
Digital inputs; SLC, FOC, RAC, CLI, 3-STATE, EN1 and EN2						
V_{IL}	LOW level input voltage	T_{amb} = –40 to +85 °C	–	–	$0.2V_{DDD}$	V
V_{IH}	HIGH level input voltage	T_{amb} = –40 to +85 °C	$0.8V_{DDD}$	–	–	V
I_{LI}	input leakage current		–	–	1	μA
Clock input; CLI						
f_{clk}	clock frequency		–	8.4672	10	MHz
Analog outputs; FO+ and FO–						
I_O	output current		–	–	250	mA
R_O	output resistance	note 2	–	tbf	4	Ω
Analog outputs; RA+ and RA–						
I_O	output current		–	–	250	mA
R_O	output resistance	note 2	–	tbf	4	Ω
Analog outputs; SL+ and SL–						
I_O	output current		–	–	560	mA
R_O	output resistance	note 2	–	tbf	2	Ω

Notes

1. Maximum supply current depends on the value of R_L: $I_{max} = \frac{V_{DDA(x)(max)}}{(R_O + R_L)}$
2. Output resistance is defined as the series resistance of the complete bridge.

Timing diagram



Sampling of the incoming data is marked by a '*'.

Fig.9 Timing diagram.

APPLICATION INFORMATION

Figure 10 shows an application example.

An LC filter is connected to each output of the SZA1010 in order to remove the PDM square wave signal at the clock frequency. This is done to prevent the relatively long wires to the actuators and motor from radiating and thereby disturbing other circuitry. Therefore it is recommended to place the coils as close as possible to the IC. The LC filter bandwidth has been chosen as high as 20 kHz to ensure that the filter's poles are far enough outside the relevant loop bandwidth, which in this application is approximately 1 kHz. In this way their influence on the closed loop performance is kept to a minimum. Furthermore, the corner frequency has not been chosen higher in order to filter out noise and spurious products as much as possible, because they enlarge the dissipation.

The various power supply and ground pins are all connected together in the schematic, but if desired, the focus, radial and sledge power pins can be connected to a separate power supply.

The three ground pins are internally connected and therefore should not be separated.

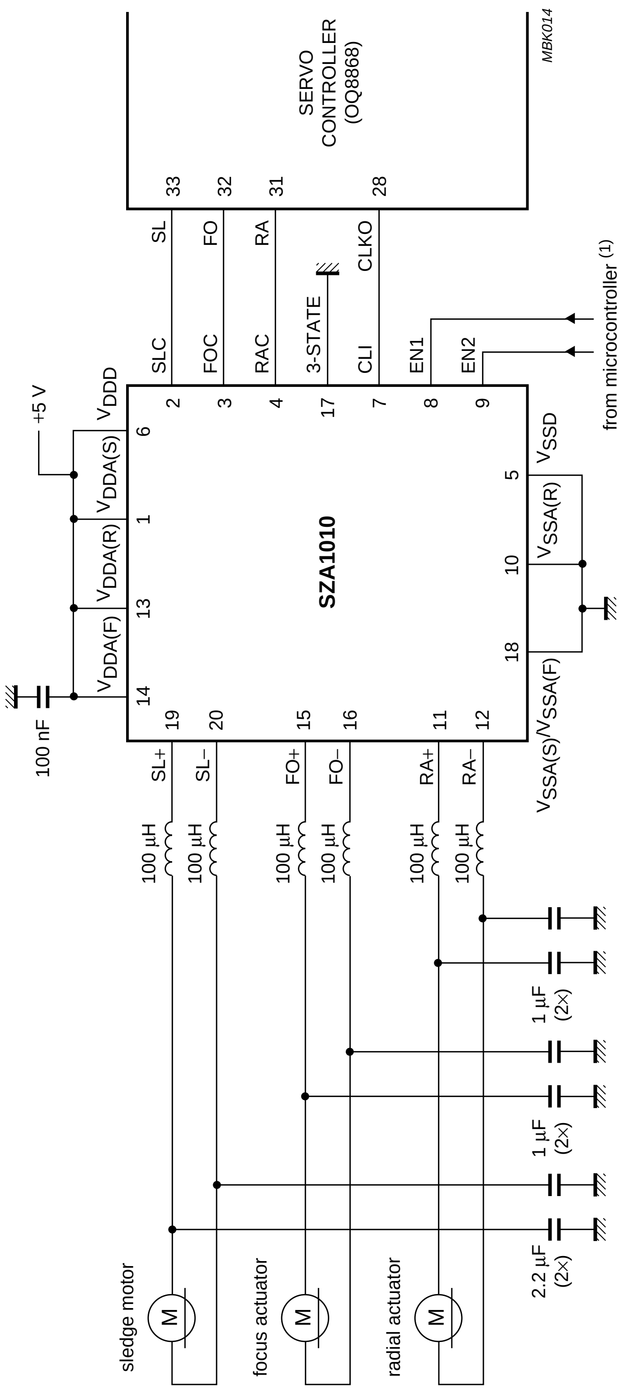
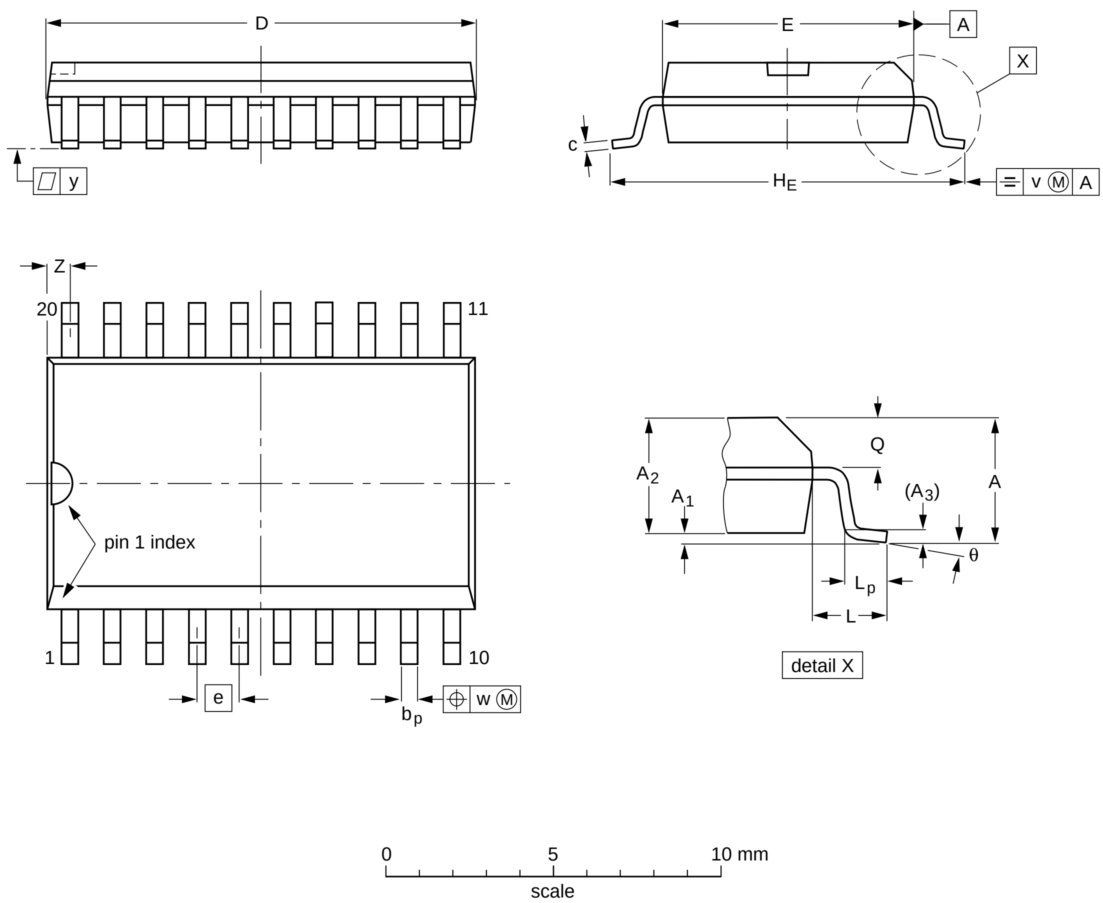


Fig.10 Application diagram.

(1) See Table 1.

PACKAGE OUTLINE

SO20: plastic small outline package; 20 leads; body width 7.5 mm SOT163-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (1)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	2.65	0.30 0.10	2.45 2.25	0.25	0.49 0.36	0.32 0.23	13.0 12.6	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8^o 0^o
inches	0.10	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.51 0.49	0.30 0.29	0.050	0.42 0.39	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT163-1	075E04	MS-013AC				~~92-11-17~~ 95-01-24

SOLDERING

Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *“IC Package Databook”* (order code 9398 652 90011).

Reflow soldering

Reflow soldering techniques are suitable for all SO packages.

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt. Dwell times vary between 50 and 300 seconds depending on heating method. Typical reflow temperatures range from 215 to 250 °C.

Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 minutes at 45 °C.

Wave soldering

Wave soldering techniques can be used for all SO packages if the following conditions are observed:

- A double-wave (a turbulent wave with high upward pressure followed by a smooth laminar wave) soldering technique should be used.
- The longitudinal axis of the package footprint must be parallel to the solder flow.
- The package footprint must incorporate solder thieves at the downstream end.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder is 10 seconds, if cooled to less than 150 °C within 6 seconds. Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

Repairing soldered joints

Fix the component by first soldering two diagonally-opposite end leads. Use only a low voltage soldering iron (less than 24 V) applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

LIFE SUPPORT APPLICATIONS

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